REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 6, 14, 16, 19 and 20 are amended. Claims 1-20 are pending in the application.

I. Information Disclosure Statement

The Examiner noted that the Information Disclosure Statement fails to comply with the provisions of 37 C.F.R. 1.97, 1.98 and MPEP § 609. An Information Disclosure Statement complying with 37 C.F.R. 1.97, 1.98 and MPEP § 609 is filed concurrently with the Amendment to the present application.

II. Objection to the Specification

The title was objected to. In light of the comments noted in the outstanding Office Action, the title is amended to "Computer System and Method for Determining Operation in a Multi-Channel Mode". Accordingly, it is respectfully requested that this objection be withdrawn.

The specification was objected to for failing to provide proper antecedent basis for the claimed subject matter. The specification was amended to provide proper antecedent basis. Accordingly, it is respectfully requested that this objection be withdrawn.

III. Rejection under 35 U.S.C. § 112

In the Office Action, at page 3, numbered paragraph 6, claims 1-18 and 20 were rejected under 35 U.S.C. § 112, 2nd as being indefinite. In light of the comments noted in the outstanding Office Action, claims 1, 6, 14 and 20 were amended. Accordingly, it is respectfully requested that this rejection be withdrawn.

IV. Rejection under 35 U.S.C. § 102

In the Office Action, at page 4, numbered paragraph 7, claims 6-9, 14, 16-17 and 19 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,003,121 to Wirt. This rejection is respectfully traversed because Wirt does not discuss or suggest:

> a controller determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses; and

> an output unit providing information whether the plurality of memory buses operate in the multi-channel mode according to the determination by the controller,

as recited in amended independent claim 6.

As a non-limiting example, the present invention is an apparatus and method for determining whether memory buses are operated in a multi-channel mode. Memory information of memory modules separated into a plurality of channels is read. A controller determines whether, based on the memory information read, memory modules in separate channels connected to separate buses can operate in a dual channel mode. That is, the memory modules in the separate channels are examined to determine whether they are mutually compatible, such that the dual channel mode can be performed. A unit displays information as to whether or not the memory buses operate in the multi-channel mode.

Wilt does not discuss or suggest "determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel," nor does Wilt discuss or suggest "an output unit providing information whether the plurality of memory buses operate in the multi-channel mode according to the determination." In contrast, Wilt discusses reading characteristics of the RDRAMs and grouping them on a channel according to the characteristics. Wilt does not discuss comparing memory information between memory modules of first and second channels to make a determination as to whether or not the characteristics of the memory modules of the separate channels are compatible, and then making a determination as to whether or not the dual channel mode may be performed. Further, Wilt makes no reference to an output unit specifically providing information as to whether the buses operate in a multi-channel mode according to the determination.

Therefore, as Wilt does not discuss or suggest "comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel" and making a determination as to "whether the plurality of the memory buses operate in the multi-channel mode," as set forth in claim 6, claim 6 patentably distinguishes over Wilt.

Regarding claims 7-13, these claims depend directly or indirectly from claim 6 and include all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 10 recites that "the output unit visually informs the arrangement of the memory modules allowing the plurality of the memory buses to

operate in the multi-channel mode." Therefore, as these claims are dependent from independent claim 6, they are believed to be allowable for at least the reasons noted above.

Claim 14 recites "comparing the read memory information of at least one of the memory modules of the first channel to the read memory information of at least one of the memory modules of at least the second channel; and outputting multi-channel mode information of the memory buses based upon the comparing." As discussed above, Wilt does not discuss or suggest comparing memory information of a memory module of a first channel to a memory module of at least a second channel and outputting information related to the multi-channel mode based on the comparison. Therefore, claim 14 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claims 15-18 depend directly or indirectly from claim 14 and include all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 16 recites that "the comparing comprises comparing memory capacities of the channeled memory modules of the first channel to at least one of the channeled memory modules of at least the second channel to determine if same memory capacity memory modules are separately connected to each memory bus, respectively." Therefore, as these claims are dependent from independent claim 14, they are believed to be allowable for at least the reasons noted above.

Claim 19 recites "outputting multi-channel mode memory bus information based upon memory information of channeled memory modules of a first channel and at least a second channel, the multi-channel mode memory bus information being determined by comparing at least one memory module of the first channel and at least one memory module of at least a second channel, the memory modules being connected to respective memory buses." As discussed above, Wilt does not discuss or suggest the features of this claim. Therefore, claim 19 patentably distinguishes over the references relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

V. Rejection under 35 U.S.C. § 103

In the Office Action, at page 9, numbered paragraph 8, claims 1-13, 17 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,845,277 B1 to Michelet et al. This rejection is respectfully traversed.

Wirt does not discuss or suggest "displaying whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information of a first memory

module to the read memory information of at least a second memory module," as recited in amended independent claim 1. Wirt does not discuss or suggest "displaying whether the memory buses operate in the multi-channel mode according to the comparing of the read memory information; and displaying an arrangement of the memory modules allowing the multi-channel mode memory bus operation," as recited in amended independent claim 20. The Examiner notes that Wirt does not teach displaying whether the memory buses operate in multi-channel mode, but indicates that Michelet makes up for the deficiencies in Wirt. The applicants respectfully submit that Michelet does not discuss or suggest "displaying whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information of a first memory module to the read memory information of at least a second memory module, " as recited in claim 1 and similarly in claim 20. Further Michelet does not discuss or suggest "displaying an arrangement of the memory modules allowing the multi-channel mode memory bus operation," as further recited in claim 20.

Michelet merely discusses displaying information relating to the BIOS version, the memory configuration and essential hardware features and parameters. Michelet does not, however, discuss displaying whether the buses operate in the multi-channel mode *by comparing the read memory information of a first memory module to the read memory information of at least a second memory module*. Michelet just displays information. Michelet does not discuss displaying an arrangement of the memory modules that would facilitate operation in the multi-channel mode.

The applicants respectfully submit that the rejection fails to establish a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). *See* M.P.E.P. § 2142.

First, as discussed above, the applicants respectfully submit that neither Wirt nor Michelet discuss all the elements of independent claims 1 and 20, which is necessary to establish a prima facie case of obviousness. Second, there is no valid motivation to combine

the references. The Examiner asserts that the combination would provide Wirt with a hardware monitoring system, which is critical for maintenance and hardware failure prevention. However, it is unclear as to how the alleged motivation would have suggested combining the grouping of memory modules in Wirt with displaying memory information in Michelet that provides an analysis of whether the buses may operate in a multi-channel mode.

In establishing a prima facie case of obviousness, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. *See* M.P.E.P. § 2142. "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." W.L. Gore & Associates v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Therefore the applicants respectfully submit that Wirt fails to discuss or suggest "displaying whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information of a first memory module to the read memory information of at least a second memory module," nor does Wirt does not discuss or suggest "displaying whether the memory buses operate in the multi-channel mode according to the comparing of the read memory information; and displaying an arrangement of the memory modules allowing the multi-channel mode memory bus operation," as recited in independent claims 1 and 20. Michelet fails to make up for the deficiencies in Wirt. Further, the applicants respectfully submit that it is impermissible hindsight to combine Wirt and Michelet, and that there is no valid motivation to combine Wirt and Michelet. Accordingly, claims 1 and 20 patentably distinguish over the references relied upon. Therefore, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 2-5 depend either directly or indirectly from claim 1 and include all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 5 recites that "the displaying whether the plurality of the memory buses operate in the multi-channel mode further comprises displaying the arrangement of the memory modules allowing the plurality of the memory buses to operate in the multi-channel mode." Therefore, as these claims are dependent on independent claim 1, they are therefore believed to be allowable for at least the reasons noted above.

Regarding the rejection of claim 6, as discussed above, Wirt does not discuss or suggest a controller "determining whether the plurality of the memory buses operate in the multi-channel

mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses," nor does Wirt discuss or suggest "an output unit providing information whether the plurality of memory buses operate in the multi-channel mode according to the determination by the controller." Michelet fails to make up for the deficiencies in Wirt. Further, the applicants respectfully submit that it is impermissible hindsight to combine the Wirt reference with the Michelet reference, and that there is no motivation to combine the Wirt reference with the Michelet reference. Accordingly, claim 6 patentably distinguishes over the references relied upon. Therefore, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 7-13 and 17 depend either directly or indirectly from claim 6 and include all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 13 recites that "the output unit comprises a monitor to display information about the arrangement." Therefore, as these claims are dependent on independent claim 6, they are therefore believed to be allowable for at least the reasons noted above.

In the Office Action, at page 16, numbered paragraph 9, claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,535,420 B1 to Kawamata. This rejection is respectfully traversed.

As discussed above, Wirt does not teach or suggest "reading memory information of at least one of a plurality of channeled memory modules of a first channel and at least one of a plurality of memory modules of at least a second channel," nor does Wirt teach or suggest "comparing the read memory information of at least one of the memory modules of the first channel to the read memory information of at least one of the memory modules of at least the second channel; and outputting multi-channel mode information...based upon the comparing." Kawamata, which discusses only that a storage area stores information such as manufacturer information, fails to make up for the deficiencies in Wirt. Accordingly, claim 6 distinguishes over the prior art. Claim 15 depends directly from independent claim 14 and includes all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. Therefore, as claim 15 is dependent on independent claim 14, it is believed to be allowable for at least the reasons noted above.

In the Office Action, at page 17, numbered paragraph 10, claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,496,945 B2 to

Cepulis et al. This rejection is respectfully traversed because, as discussed above, Wirt does not discuss or suggest the features of independent claim 6. Cepulis, which discusses a north bridge device coupling CPUs and memory modules, fails to make up for the deficiencies in Wirt. Accordingly, claim 6 distinguishes over the references relied upon. Claim 18 depends indirectly from independent claim 6 and includes all the features of that claim, plus additional features that are not discussed or suggested by the references relied upon. Therefore, as claim 15 is dependent on independent claim 6, it is believed to be allowable for at least the reasons noted above.

Conclusion

In accordance with the foregoing, the specification and claims 1, 6, 14, 16, 19 and 20 have been amended. Claims 1-20 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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